WHAT IS CLAIMED IS:

1. A method of digitizing first and second signals in imperfect quadrature for obtaining characteristic parameters of the first signal, the method comprising:

providing a first signal, the first signal comprising an inphase quasi-sinusoidal analog signal;

providing a second signal, the second signal comprising a quadrature signal;

digitizing the first signal at a sampling rate, thereby generating a first plurality of sets of digital signal waveform samples;

digitizing the second signal at the sampling rate, thereby generating a second plurality of sets of digital signal waveform samples; and

digitally processing successive first and second sets of digital signal waveform samples to generate continually updated digital characteristic parameters representing a characteristic behavior of the first signal.

2. The method of claim 1, wherein the digital characteristic parameters comprise a phase progression of the first signal.

3. The method of claim 1, wherein the digital characteristic parameters comprise a phase-offset correction of the first signal.

4. The method of claim 1, wherein the digital characteristic parameters comprise a magnitude estimate of the first signal.

5. The method of claim 1, wherein the digital characteristic parameters comprise a frequency estimate of the first signal.

6. The method of claim 1, wherein each first and second sets of digital signal waveform samples include integer power of 2 number of samples.

7. The method of claim 1, wherein the sampling rate is 80 MHz.

8. The method of claim 1, wherein the step of digitally processing successive first and second sets of digital signal waveform samples further comprises:

generating a first best-fit estimate of the first signal for each first set of digital signal waveform samples; and

generating a second best-fit estimate of the second signal for each second set of digital signal waveform samples.

9. The method of claim 8, wherein the best-fit estimate of the first signal is determined by an equation $V*\cos[2\pi(Freq*i-\theta)]$, wherein i is an index for identifying consecutive digital signal waveform samples within a set, V represents a magnitude estimate, $Freq$ represents a frequency estimate, and θ represents a phase-offset estimate.

10. The method of claim 8, wherein the best-fit estimate of the second signal is determined by an equation $U*\sin[2\pi(Freq*i-\theta+\Delta\theta)]$, wherein i is an index for identifying consecutive digital signal waveform samples within a set, U represents a magnitude estimate, $Freq$ represents a frequency estimate, θ represents a phase-offset estimate, and $\Delta\theta$ represent a phase error.

11. The method of claim 1, wherein the step of digitally processing successive first and second sets of digital signal waveform samples is based on a block regression technique, wherein linear regression processing is applied to selected sums of the digital signal waveform samples.

12. The method of claim 1, wherein the frequency of the first signal is outside a range of approximately -300 kHz to +300 kHz.

13. The method of claim 12, wherein the step of digitally processing successive first and second sets of digital signal waveform samples further comprises:

calculating calibration factors magnitude ratio $|V/U|$ and phase error $\Delta\theta$ to use in digitally processing successive first and second sets of digital signal waveform samples if a frequency of the first signal moves to within a range of approximately -300 kHz to +300 kHz, where V is the magnitude of the first signal and U is the magnitude of the second signal.

14. The method of claim 1, wherein a frequency of the first signal is within a range of approximately -300 kHz to +300 kHz.

15. A phase digitizing system comprising:

a first analog-to-digital converter for generating a first plurality of segments of digital signal waveform samples based on an incoming first signal;

a second analog-to-digital converter for generating a second plurality of segments of digital signal waveform samples based on an incoming second signal;

a digital phase accumulator; and

a digital signal processor coupled to the first and second analog-to-digital converters and the digital phase accumulator for digitally processing each first and second segments of the digital signal waveform samples together with an output of the phase accumulator and for continually generating digital phase data, the digital signal processor configured to provide increment values to the digital phase accumulator based on the digital phase data, thereby causing the output of the digital phase accumulator to represent an instantaneous phase of the incoming first signal.

16. The phase digitizing system of claim 15, wherein the digital phase data includes a phase correction value.

17. The phase digitizing system of claim 15, wherein the digital phase data includes a frequency update value.

18. The phase digitizing system of claim 15, wherein the digital phase data includes a magnitude estimate of the incoming first signal.

19. The phase digitizing system of claim 15, wherein the digital phase data includes a magnitude estimate of the incoming second signal.

20. The phase digitizing system of claim 15, wherein each first and second segment of digital signal waveform samples includes a number of digital signal waveform samples equaling an integer power of 2.

21. The phase digitizing system of claim 15, wherein the first and second analog-to-digital converters generate digital signal waveform samples at 80 MHz.

22. The phase digitizing system of claim 15, wherein the incoming first signal is an inphase signal.

23. The phase digitizing system of claim 15, wherein the incoming second signal is a quadrature signal.

24. The phase digitizing system of claim 15, wherein the digital phase accumulator is configured to generate a plurality of digital phase progression values based on current frequency values and current phase correction values, each digital phase progression value including a whole number portion and a fractional number portion.

25. The phase digitizing system of claim 24, wherein the digital signal processor further comprises:

a first cosine table coupled to the digital phase accumulator for providing cosine values corresponding to the fractional number portion of the digital phase progression values;

a first sine table coupled to the digital phase accumulator for providing sine values corresponding to the fractional number portion of the digital phase progression values;

a first plurality of arithmetic logic units (ALUs) for arithmetically processing the first cosine values and the first sine values, each ALU in the first plurality of ALUs configured to output a result value based on the arithmetic processing; and

a second plurality of ALUs coupled to the first analog-to-digital converter for arithmetically processing the first digital signal waveform samples, each ALU in the second plurality of ALUs configured to output a result value based on the arithmetic processing,

wherein the digital signal processor is configured to generate the current phase correction values based on the result values output by the first and the second plurality of ALUs, and configured to generate each current frequency value based on a current digital phase value and a plurality of past digital phase values.

26. The phase digitizing system of claim 25, further comprising:

an adder coupled to the digital signal processor, the adder configured to provide feedback to the digital signal processor to correct for phase error.

27. The phase digitizing system of claim 26, wherein the digital signal processor further comprises:

a second cosine table coupled to the adder for providing cosine values corresponding to the fractional portion of the digital phase progression values modified by a phase error;

a second sine table coupled to the adder for providing sine values corresponding to the fractional portion of the digital phase progression values modified by a phase error;

a third plurality of arithmetic logic units (ALUs) for arithmetically processing the second cosine values and the second sine values, each ALU in the

third plurality of ALUs configured to output a result value based on the arithmetic processing; and

a fourth plurality of ALUs coupled to the second analog-to-digital converter for arithmetically processing the second digital signal waveform samples, each ALU in the fourth plurality of ALUs configured to output a result value based on the arithmetic processing,

wherein the digital signal processor is configured to generate the current phase correction values based on the result values output by the first, second, third and the fourth plurality of ALUs, and configured to generate each current frequency value based on a current digital phase value and a plurality of past digital phase values.

28. The phase digitizing system of claim 27, wherein the digital signal processor further comprises:

a plurality of registers coupled to the ALUs for storing the result values.

29. The phase digitizing system of claim 28, wherein the digital signal processor further comprises:

a latch coupled to the digital phase accumulator for latching a digital phase progression value.

30. The phase digitizing system of claim 29, wherein the digital signal processor further comprises:

a counter coupled to the plurality of registers and the latch, the counter configured to cause the registers to store the result values at an end of each segment of first and second digital signal waveform samples, the counter configured to cause the latch to latch a phase progression value substantially near a center of each segment of first and second digital signal waveform samples.

31. The phase digitizing system of claim 30, wherein the digital signal processor is configured to generate each current digital phase value by

subtracting a current phase correction value from the latched phase progression value.

32. A displacement measuring interferometry system comprising:

a light source for generating at least one light beam;

an interferometer for generating an optical measurement signal based on the at least one light beam;

optics for generating a quadrature optical measurement signal based on the optical measurement signal;

a receiver for receiving the quadrature optical measurement signal and an optical reference signal, the receiver configured to generate an analog measurement signal based on the quadrature optical measurement signal and configured to generate an analog reference signal based on the optical reference signal;

at least two analog-to-digital converters for generating a first plurality of sets of digital measurement signal waveform samples based on an inphase portion of the measurement signal, and for generating a second plurality of sets of digital measurement signal waveform samples based on a quadrature portion of the measurement signal, the at least two analog-to-digital converters configured to generate a plurality of sets of digital reference signal samples based on the analog reference signal; and

at least one digital signal processor coupled to the at least two analog-to-digital converters for digitally processing each first and second set of the digital measurement signal waveform samples and the digital reference signal waveform samples, the at least one digital signal processor configured to generate digital measurement phase data representing an instantaneous phase of the analog measurement signal, the at least one digital signal processor configured to generate digital reference phase data representing an instantaneous phase of the analog reference signal.

33. The displacement measuring interferometry system of claim 32, wherein the optics for generating a quadrature optical measurement signal further comprises:

a non-polarizing beam splitter for splitting the at least one light beam into a first light beam and a second light beam, the at least one light beam, first light beam, and second light beam comprising first and second frequency components orthogonally linearly polarized;

a quarter wave plate in the path of the first light beam, the quarter wave plate for changing the orthogonally linearly polarized light to orthogonally circularly polarized light;

a first polarizer in the path of the first light beam, the first polarizer for changing the orthogonally circularly polarized light to linearly polarized light; and

a second polarizer in the path of the second light beam, the second polarizer for changing the orthogonally linearly polarized light to linearly polarized light.

34. The displacement measuring interferometry system of claim 33, wherein a fast access of the quarter wave plate is set at approximately 45 degrees to the orthogonally polarized components in the first light beam.

35. The displacement measuring interferometry system of claim 33, wherein a polarizer axis of the first polarizer is oriented at approximately 45 degrees to a fast access of the quarter wave plate.

36. The displacement measuring interferometry system of claim 33, wherein a polarizer axis of the second polarizer is oriented at approximately 45 degrees to the orthogonally polarized components in the first light beam.

37. The displacement measuring interferometry system of claim 33, wherein a phase difference between the linearly polarized light of the first light beam

exiting the first polarizer and the linearly polarized light of the second light beam exiting the second polarizer is approximately 90 degrees.

38. The displacement measuring interferometry system of claim 32, wherein the digital measurement phase data represents a phase progression of the analog measurement signal, and wherein the digital reference phase data represents a phase progression of the analog reference signal.

39. The displacement measuring interferometry system of claim 32, wherein the digital processing performed by the digital signal processor is based on a block regression technique, wherein linear regression processing is performed on sums of digital signal waveform samples.